

CHAPTER 6

HIGH TEMPERATURE ELECTRONICS PACKAGING IN EUROPE

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INTRODUCTION

To understand the meaning of high temperature electronic packaging one would have to have a clear understanding of high temperature electronics in general. High temperature electronics may be defined as those devices and/or subsystems that operate at elevated temperatures above 200°C. Similarly high temperature electronic packaging may be defined as establishing interconnections and a suitable operating environment for these electronic devices (e.g., SiC, GaN or Si) at temperatures above 200°C. These definitions can be argued as too vague or inadequate since many researchers have varying opinions on what constitutes high temperature (i.e., electronics operating above 300 °C, above 400 °C, etc.). However, most researchers would agree that there needs to be significant consideration given to addressing both the components and packaging needs for high temperature applications to achieve similar levels of integration and functionality to what is currently being practiced at ambient and near ambient conditions for today's silicon and III-V compound IC's.

Most high temperature applications will find their niche in harsh environments, such as under the hood for exhaust gas sensors and in exposed areas of an aircraft. Applications such as these may be impractical for conventional silicon, unless one introduces highly complex and expensive packaging techniques involving liquid cooling, etc. Although these are very important issues to address, many in the silicon IC world are very reluctant to make the necessary investments to produce the high quality devices necessary to meet these challenges. As a result, the electronic packaging community, which is under tremendous pressure to find low cost solutions to package IC's, will also be slow to address the packaging needs for high temperature applications. In addition to business pressures and challenges, there are also significant technical challenges to package wide band gap materials for high temperature applications.

To package wide band gap materials for high temperature applications a number of alternative materials, including substrates and solders, and fabrication techniques have to be considered over conventional packaging practices. Today most devices are packaged using glass epoxy boards and organic encapsulants. At the temperatures of interest in this study, these components would melt or significantly degrade thermally, thus proving impractical for use. Eutectic solders as well as conventional die attach materials will also need to be addressed. Passive device selection and reliability testing are also critical issues as well.

The following chapter will address some of these issues as they were discussed during the TTEC sponsored study on "High Temperature Electronics in Europe". I should caution however, the amount of interaction was very limited for this subject matter, as many of the researchers whom the team visited were not directly involved in electronic packaging and had little knowledge regarding plans and future directions for the packaging of their devices. However, some were knowledgeable, including experts at Siemens and IMC. It is therefore our intention to present in this chapter their views as well as some of the views of the author on

the status and direction for some key technology elements of packaging for some high temperature applications involving SiC, GaN and Si.

PASSIVE DEVICE SELECTION

A critical question in the packaging of high temperature electronics is what do you do about the passive components? Two of these components involve resistors and capacitors. Since there is a component of resistivity which can be expressed as function of temperature due to lattice vibrations (or phonons) it stands to reason that one must exercise care when laying out their designs, for instance for a MCM which may utilize high temperature devices. An important characteristic for resistor components is its TCR or Temperature coefficient of resistivity. If the TCR of a resistor is properly characterized and quantified then it should not cause premature failure of a system or parameter drifts, since it can be addressed by careful circuit design that balances the characteristics of several resistors to create a network unaffected by temperature (Pecht 1994). However, other factors such as humidity, stress, etc. can alter the performance of a resistor depending upon the material choices. Table 6.1 shows the TCR for some common resistor materials.

Table 6.1

TCR for Common Resistor Materials (Pecht and Lall 1994; Elshabini-riad 1991; Heidler 1969)

<i>Resistor Types</i>	<i>Max Operating Temp (°C)</i>	<i>TCR (ppm/K)</i>
Wirewound resistor		
Precision	145	10
Power	275	260
Metal-film resistor		
Precision	125	50-10
Power	165	20-100
Composition resistor		
General Purpose	130	1500
Deposited resistor		
Thin Film		
Tantalum	>200	+/-100
Tantalum Nitride	>200	-85
Titanium	>200	+/-1000
SnO ₂	>200	-1500 to 0
Ni-Cr	>200	+/-100
Cermet		+/-150
Thick Film		
Ruthenium silver	>200	+/-200

Palladium silver	>200	-500 to 150
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On the other hand, capacitors are very difficult to design for in high temperature applications since the dielectric constant and the loss tangent will fluctuate with increasing temperature. Typically designers will use either polymer film dielectric materials, thin films, or ceramic materials. Table 6.2 illustrates some of the material choices and their properties for high temperature polymers.

Table 6.2

Dielectric Film Candidates for Elevated Temperature Wound Capacitors (McCluskey 1997)

Dielectric Material	Commercial Source	Properties and Advantages
Polysilsequioxane	David Sarnoff Labs	Good electrical properties up to 250C
Teflon Perfluoroalkoxy	DuPont	Good mechanical and electrical properties up to 200C
Polyimide	DuPont	Small variations in dielectric loss up to 200C
PBO	Foster-Miller, Dow	Good temperature stability, 300 to 350C
PBO-flourinated IPN	Foster-Millier	High temperature stability
Organo-ceramic hybrid nano composites	Garth Wilkes, VPI	Resistant to ionizing radiation; high thermal stability
Polybenzimidazole	Hoechst Celanese	Thermoplastic; excellent thermal stability above 300C
Flourinated PBO-PI	Hoechst Celanese	Combines polyimides with high temperature properties of LCP's

Thin films will also have a place when there is a need to integrate capacitors either onto high temperature electronic packages, or off chip as it is sometimes referred. A number of dielectric materials have been deposited in the form of thin films using techniques like MOCVD (Stauf 1998; Nami 1997), PECVD (Trigg 1998; Lenihan 1996), Anodization (Nelms 1998), Sputtering (Kapadia 1998; Kim 1998; Tsukada 1995; Simamoto 1992; Vorotilov 1999; Suu 1998), Hydrolysis (Sakabe 1998), and PLD (O'Neill 1998; Noda 1999) etc.

Recently there has been a tremendous amount of interest in deposition of inorganic thin films using the sol-gel method. Very thin films of perovskite materials like BaTiO₃ or Lead based relaxor ferroelectrics have been fabricated by Vorotilov et al. to yield capacitance densities as high as 7 –9 $\mu\text{F}/\text{cm}^2$.

Table 6.3**Some selected ceramic candidates for high temperature capacitors**

Industry/Institution	Materials	Approach	Highest ϵ_r Achieved	Highest C (nF/cm ²)	Reference
Cornell University	Polymer/ceramic	Collodial dispersion	40		[Liang98]
TPL Industries	Nanocomposites	Surface treatment		25	[Slenes98]
3M Corporation		Roll to roll process		10	[O'Bryan98]
Georgia Institute of Technology		Dispersion control	135	22	[Agarwal98]
IBM		Conventional mixing	47		[Levy98]
Chalmers University of Tech, Sweden	Polymer/BaTiO ₃ /Carbon	Conventional mixing	1960		[Ardi97]
Ormet Corporation		Dry film/curtain coating	40	4	[Brandt98]
Institute for surface chemistry, Sweden	Nanocomposites	Dispersion optimization			[Bergstrom97]
Matsushita Electric Works	Polyphenyleneoxide-TiO ₂	Lacquered film-gravure coat	12		[Simamoto92]
Sandia National Laboratories	PZT and PLZT	Sol-gel	900		[Dimos94]
University of Delhi, India	BaTiO ₃		370		[Sharma98]
Princeton University	Hydrothermal BT	Organo-metallic precursors			[Slamovich96]
Hitachi Res. Lab., Hitachi Ltd., Japan	Ta _x O _y	Sol-gel; Photo Irradiation	28		[Ohishi92]
Electr.&Automation(Tech.Univ),Russia	PZT, SrBiTa Oxide films	Sol-gel	1000	7000-9000	[Vorotilov99]
Nanyang Tech. University, Singapore	Ba-Ti-B Ceramic Glass	Sol-gel, thick film		2500	[Yao98]
AVX Corporation	PbZT	Sol-gel			[Liu99]

European Input on Passive Device Selection

Unfortunately there was very little discussion on this study tour on passive device selection for high temperature applications. All who spoke were in agreement that much more work needs to be done in this area. Dr. Roumen Kakanakov of the Institute of Applied Physics in Bulgaria indicated that his team had a little experience with passive integration as well as passive component attachment using high temperature solders.

FIRST LEVEL PACKAGING

In this section we will consider some major elements of first level packaging that require serious consideration when packaging devices at elevated temperatures. These are the technology elements, which were discussed with the European researchers. For first level packaging we will only consider wirebond, die attach materials and contact metallization. Other issues such as encapsulants, hermetic lids, and C4 will not be discussed.

Wirebond

Connections between the IC device and the electronic package are commonly performed by one of three technologies: wirebond, solder, or controlled collapsed chip connection (C4). Of the three technologies, wirebond will be discussed here because it is the most prevalent and cost effective of the three and is being practiced by the Europeans as the desired interconnection method for connecting the wideband gap devices to the package. It should also be noted that wirebonding concurrently provides for thermal dissipation by backbonding or diebonding the chip to the substrate, as illustrated in Figure 6.1. This configuration allows for the designer to utilize some of the more thermally conductive substrates to facilitate heat removal from the backside of the die. However, the designer must also keep in mind that with wirebond, he or she will pay a price for lead inductance.

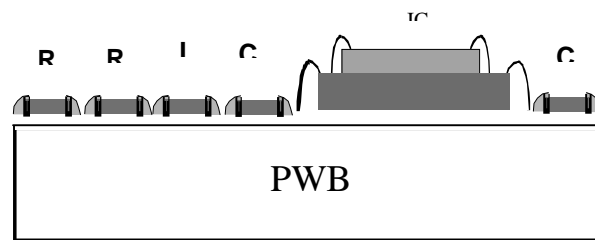


Fig. 6.1. Schematic representation of a wideband gap IC device mounted on a substrate and connected to it using wirebonds, which in turn is mounted to a PWB motherboard and connected by wirebonds.

Another critical factor that one must consider when operating at an elevated temperature is the material interactions that will occur between the wire and the pad to which it is being bonded to. Most high temperature applications tend to use aluminum wire to aluminum contacts. This particular union can withstand temperatures up to 600°C. Gold to gold bonding is also very reliable and can withstand temperatures up to 1000°C. Designers should try to avoid bonding dissimilar metals such as Al to Au or Cu to Al, because of the brittle intermetallic phases that could form at elevated temperatures, which could thereby cause premature failures at the interface (Newsome 1976).

The researchers at Siemens, led by Professor Eckhard Wolfgang, were well aware of these concerns. They shared with us a six-chip multichip module that was being used in the braking system of a locomotive engine. Each locomotive would require 18 to 24 modules and would operate at temperatures between 110°C and 125°C. The module contained six thyristors that had 30 to 40 I/Os per chip and were wirebonded using aluminum wire to aluminum contacts. Professor Wolfgang's focus is in applications below 200°C.

In France, the researchers at LETI also showed us a packaged device, which was wirebonded onto a lead frame that they believed to be made of Mo-Cu. The researchers there did not know much detail regarding this package, since they outsource their packaging. We were later told the package was procured from Dr. Kakanakov of Bulgaria. It was unclear who performed the wirebonding.

Die Attach

Another critical element in the packaging of high temperature electronic devices is the die attach material. The die attach material is used to ensure that the device remains in place throughout the entire lifetime of the

system. The die attach material should also have good thermal conductivity, as well as good contact resistance. There are a number of die attach materials, which have inherent advantages and disadvantages depending on the temperature of operation of the device. Table 6.4 displays temperature guidelines for a select number of die attach materials.

Table 6.4

Temperature guideline for Some Die Attach Materials (Manko 1992; Pecht 1994; Feinstein 1989; Khatchatourian 1995; Olson 1995)

Die attach material	Maximum use temperature	Reason
Au80Sn20	280°C	Eutectic melting point
Au88Ge12	356°C	Eutectic melting point
Au97Si3	363°C	Eutectic melting point
Sn96Ag4	221°C	Solidus
Sn95Sb5	235°C	Solidus
Sn92Sb8	236°C	Solidus
Sn65Ag25In10	236°C	Liquidus
Polyimide	300°C	Glass transition temperature
Silver filled glass	450°C	Softening point

In Europe, significant input on die attach materials was provided by Dr. Kakanakov. The following is a summary of our discussion relative to die attach materials and his rationale for material selection. After completion of this project in 1997, Kakanakov continued to make a small series of packages for power SiC MESFET'S from Thomson CSF. In early 1999 work began on the NATO project "High Power and High Frequency Devices on LPE-grown SiC films", where Kakanakov's group was responsible for R&D of packages and packaging of power SiC diodes (Kakanakov 1999). Two gold-based alloy materials were used as attach materials. The attach materials were gold based alloys of Au and (6%) Si, (12%) Ge. The 6% alloy has a melting point of 373°C, and the 12% alloy melts at 363°C. Kakanakov mentioned (but did not go into great detail) that his group also investigated AuSn (20%) alloy and an AuIn (25%) alloy which had a melting point of 450°C. The AuIn system exhibited a favorable melting point but there was significant concern regarding the oxidation of In at the high temperatures.

Contact Metallization

The contact metallization is very critical as it serves a number of purposes such as providing a wetting layer for the die attach material, as well as ensuring optimal adhesion between the device and the die attach material. The contact metallization should be resistant to oxidation and be thermally stable at elevated temperatures. Typically this metallization is accomplished in a multilayering arrangement. The first metal layer is usually an adhesive layer, typically Cr or Ti. The second layer in this metal stack is usually referred to as the barrier layer metal. It serves to protect the adhesive layer. Typical barrier metals may be Ni, Ni alloys, Co, Co alloys, Pt and phased CrCu alloys. The third layer is typically called the wetting layer. This layer allows for wetting of the die attach alloys to ensure a reliable contact. Work by Kakanakov showed that the contact metallization of TiPtAu was suitable for SiC MESFET devices up to joining temperatures of 400°C. The advantages here were that there was no change in thermal resistance during high temperature testing. However, Pt and Ti will dissolve in both of the solders when it is liquified, thereby indicating that more suitable barrier metallurgies will have to be identified at the temperature extremes. Kakanakov et al indicated that the solders used in this study were only in liquid state during chip attachment and not during actual device operation. To limit the solubility of their barrier metallization of platinum and increase

adhesion, a new process was developed in their laboratories. The new process involved vibrating the device during attach. This resulted in a reduction of the bonding time and reduced dissolution of the Pt in the Au alloy solders, thereby enhancing adhesion and improving reliability. No additional details were given. Gold wiring bonding is performed using a ball bonder from K&S when making connections from the chip to the second level of packaging, the substrate. The substrate in this case is made of a CuMo alloy.

SECOND LEVEL PACKAGING

Second level packaging includes substrates, solders, connectors, housing and cables. However, in this section we will only discuss substrates and briefly mention solders since our discussions in Europe were limited to these areas. Dr. Kakanakov and Professor Wolfgang of Siemens provided the majority of the input from Europe for this section.

As mentioned earlier plastic substrates such as glass reinforced epoxy boards may not be satisfactory due to its low T_g and melting point. However, many designers are looking to a new class of organic boards called BT Resins, which offer the opportunity to meet some of the high temperature requirements just above 200°C. Although these organic materials have a fairly high T_g, they still are poor conductors of heat and therefore will require intricate cooling schemes to efficiently remove heat. Also organic materials such as BT resins will provide challenges from a thermal mismatch standpoint because of its large CTE > 17ppm/°C and polyimide another high temperature organic, which has a CTE of > 30ppm/°C. These materials may warrant consideration because of their low cost nature and the ability to procure them in bulk quantities.

On the other hand, there are a number of inorganic candidates, which should be satisfactory, both from a performance and cost standpoint to meet the needs of most of these high temperature applications. A leading candidate would certainly have to be ceramic substrates. Ceramics have typically been used for a number of high temperature applications such as Al₂O₃, AlN and glass ceramic. The majority of high temperature packaging, including the majority of automotive under the hood applications, consists of thick film hybrid cermet and ceramics (Aday 1993). One drawback of the ceramic however, is its thermal conductivity and its high cost relative to organics. DuPont addressed these cost issues with the introduction of their low temperature co-fired ceramic (LTCC) material. Here layers of unfired or "green tape" materials are circuitize and laminated to form a circuit and then simultaneously fired to form the final product at a low temperature.

Other inorganic substrate materials include silicon and metal alloys, such as Mo-Cu. Here one is afforded the ability to closely match the CTE of the high temperature device. However, there is one inorganic material, which has almost all of the desirable properties from a mechanical standpoint. That material is diamond, although cost remains a question mark (Tummala, 1989).

Another class of materials that may warrant consideration from a substrate standpoint are composites. These composites include fiber and particle reinforced metals and polymers as well as metal matrix composites. Because of the large amount of potential combinations of materials that may be suitable candidates, a summary of these materials is presented in Table 6.5.

Table 6.5**Potential composite material candidates**

Fibers	Advantages or Disadvantages
Carbon	Inexpensive, Good thermal properties
Aramid	Good CTE match
High density polyethylene	Limited temperature capability
PBO, PBT, PBZT	Environmental out of favor now
Particles	
Silicon Carbide	Tailor CTE, good thermal
Aluminum Nitride	Tailor CTE, good thermal
Cubic Boron Nitride	
Matrices	
Aluminum	Lightweight, good thermal, CTE match
Cu	Lightweight, good thermal

At Siemens, Professor Wolfgang utilized ceramic substrates for the locomotive application. At IMC in Sweden, we were informed that ceramic substrates were also being used and being considered for gas sensor applications. At the University of Ulm, diamond substrates were being considered to package GaN devices, and in Bulgaria, Dr. Kakanakov is working with Mo(40%)Cu(60%) alloy substrate. It should also be mentioned here that Dr. Kakanakov is supplying a majority of the packaging for the SiC and GaN devices in Europe. It appears that the MoCu alloy that he is working with has been very well characterized and appears to perform well in reliability testing. The CTE of this alloy ($\alpha = 3.5 \times 10^{-6}/K$) is very close to that of SiC which is ($\alpha = 4.2 \times 10^{-6}/K$). The thermal conductivity of this alloy is also very good, with $k = 245 \text{ W/mK}$.

Solders

I will briefly touch upon solders for high temperature applications. Solders are used for making connections from the device to first level packaging via C4 technology and connecting first level packaging to second level packaging via ball or stud grid array and in surface mount technology (SMT). In conventional packaging, eutectic Pb/Sn solders have been the primary workhorse for solder connections. However, for high temperature applications above 300°C this solder may not be satisfactory. Another force against Pb based solders is the drive towards green packaging technologies, or environmentally friendly materials, which precludes the use of Pb based solders in electronic applications. Materials currently receiving considerable attention as potential replacements to Pb/Sn solders include AgSn, AuSn, Cu, Sb and Bi as ternary alloys. High temperature conductive adhesives are being considered as well.

Reliability

We have listed a number of technical challenges and issues in the earlier sections of this chapter confronting the development and implementation of electronic packaging for high temperature devices. Another significant concern manifests itself in the ability to perform meaningful reliability testing, and data interpretation. A chief concern here is that there really does not exist an infrastructure for high temperature reliability testing. Most of the test equipment and chambers are set up for conventional package reliability testing and therefore only cover a limited temperature range. All of the European researchers who are

actively involved in packaging also realize that this is a valid concern, and are exploring means to fill this void. Professor Wolfgang of Siemens indicated that there is a real need to perform extended life cycle tests out to 35 years due to the fact that some products will have to survive in the field with no failures for that long. Siemens has also put a task force in place (RAPSDRA) to identify failures and failure mechanisms through accelerated testing, and develop a set of standards for power electronics that correspond to a 35 year life cycle. In addition Siemens is pursuing the following to gain more understanding on the reliability of their electronic packages at elevated temperatures of operation:

- Siemens would like built in reliability (monitor process parameters and materials)
- Developing standardization for accelerated testing (100x)
- Monitor operation of devices in real time (in-situ) using optical fibers
- Explore the theoretical limit for Si device operation (may be higher than 250°C)

Siemens has also developed reliability models that can be downloaded from their website at www.infineon.com "SFET".

Dr. Kakanakov agrees that new reliability test equipment and methodologies may be needed for high temperature reliability assessment. Limited reliability data exists for some of his systems; however, some reliability studies were done using thermal resistance measurements. An important need for the advancement of high temperature electronic packaging will be the advent of better reliability modeling and simulation tools over and above what is currently being used today.

SUMMARY

I have tried to convey some of the challenges for the packaging of high temperature devices such as GaN and SiC. These challenges are not insurmountable and will be overcome when the proper resources are put into place to address specific areas. It appears that the Institute of Physics in Bulgaria, as well as Siemens in Germany are addressing a number of these issues already and have made significant progress in finding potential solutions for some applications. Of course there are a number of vertically integrated companies around the world, which have found solutions to most of the high temperature applications but at a cost premium. Here the challenge is to find similar cost performance packaging solutions for high temperature applications much like that of conventional Si IC packaging.

REFERENCE

J. Aday, R.W. Johnson, J.L. Evans, and C. Romanczuk, "Thick Film Silver Multilayers for Under-the-Hood Applications", Proc. Int. Symp. On Microelectronics, ISHM, 1993 pp126-131.

V. Agarwal, P. Chahal, R. Tummala, and M. Allen, "Improvements and recent advances in nanocomposites capacitors using a colloidal technique", IEEE 48th Electronic Components and Technology Conference, p 165.

L. Brandt, "New materials for embedded passive components", PAN Pacific Microelectronics Symposium Proceedings, IMAPS, 1998, pp 195-199.

L. Bergstorm, K. Shinozaki, H. Tomiyama and N Mizutani, "Colloidal Processing of a Very fine BaTiO₃ Powder – Effect of Particle Interactions on the Suspension Properties, Consolidation, and Sintering Behavior", J. Am. Ceram. Soc., 80 [2], (1997), p 291 –300.

D. Dimos, S. J. Lockwood, and M. Rodgers, "Thin film decoupling capacitors for multichip module", IEEE, 1994, pp 894-899

L. Feinstein, Die Attachment Methods, Electronic Materials Handbook, Vol. 1 Packaging, ASM International, Materials Park 1989.

R. Kakanakov, L. Kassamakova, G. Sarov, U.S. Europe Conference on Wide Bandgap Semiconductor Technology for Next Generation Electronic and Photonic Devices, Arlington, Va 1999

H. Kapadia, H. Cole, M. Nielsen, N. Krishnamurthy, "Necessary characterization of integral passives for high performance applications", Integrated Passive Advanced Technology Workshop, Denver, 1998.

T. Lenihan, L. Schaper, Y. Shi, G. Morcan and J. Parkerson, "Embedded thin film resistors, capacitors, and inductors in flexible polyimide films", 46th Electronic Components and Technology Conference, 1996, pp 119-124

F. Levy, "High dielectric loaded films", Advanced Materials & Manufacturing Processes, 1988, pp 309-326

S. Liang, S. Chong, E. Giannelis, "Barium titanate/epoxy composite dielectric materials for integrated thin film capacitors", 48th ECTC, 1998, pp 171-175.

D. Liu, R. Kennedy, G. Korony, S. Makl, J. Mevissen, J. Hock and R. Heistand, "Integrated thin film capacitor arrays", Proc SPIE Int Soc Opt Eng ,3830, (1999), p 431-437.

H. Manko, Solders and Soldering, 3rd. ed., McGraw-Hill, N.Y. 1992, p116

B. Martin, C. Basceri, S. Strifer and A. Kingon, "Electrical properties of integrated Ta₂O₅ metal-insulator-metal capacitors", Electrically Based Microstructural Characterization II Mater. Res. Soc. Symp. Proc.,500, (1998), p 101-106

F. McCluskey, R. Grzybowski, and T. Podlesak, "High Temperature Electronics", CRC Press, Inc., N.Y., 1997

Z. Nami, O. Misman, A. Erbil, G. S. May, "Computer simulation study of the MOCVD growth of titanium dioxide film", J. Crystal Growth, 171 (1997) 154-165.

D. Nelms, R. Ulrich, L. Schaper and B. Bowen, "Fabrication and performance of integrated capacitors on silicon and flexible substrates", Proc SPIE Int. Soc. Opt. Eng., 3582, (1998), p. 441-446.

M. Noda, H. Sugiyama and M. Okuyama, "Study on a metal-ferroelectric-oxide-semiconductor structure with thin silicon oxide film using SrBi₂Ta₂O₉ ferroelectric films prepared by pulsed laser deposition", Jpn. J. Appl. Phys. Part 1 Regul. Pap. Short Note Rev. Paper, 38, 9, (1999), p. 5432-5436.

N. O'Bryan, "Making embedded capacitors by roll-to-roll process", IMAPS Integrated Passive Advanced Technology Workshop, Denver, 1998.

D. O'neill, G. Catalan, F. Porras, R. M. Bowman and J. M. Gregg, "Thin film ferroelectric for capacitor applications", J. of Materials Science, Materials in Electronics, 9, (1998), p 199-205.

T. Ohishi, S. Maekawa and A. Katoh, "Synthesis and properties of tantalum oxide films prepared by the sol-gel method using photo-irradiation, J. of Non-Crystalline Solids, 147 & 148, (1992), 493-498.

M. Pecht, P.Lall, Passive components of the Electrical Engineering Handbook, R.C. Dorf, ed., CRC Press, Boca Raton, Fl. 1994 p 5-15

E. J. Rymaszewski, T.M. Lu, M. C. Nielsen, J.-Y. Kim, "Integrated Discrete Components", 193rd Meeting of the Electrochemical Society, San Diego, CA, May 1998.

Y. Sakabe, N. Wada, J. Ikeda, and Y. Hamaji, "Ceramic for Ultra-thin Dielectric Layer of Multilayer Ceramic Capacitors", IEEE Int. Symp. Appl. Ferroelectrics, 1998,p 565-569.

H. B. Sharma and A. Mansingh, "Sol-gel processed barium titanate ceramics and thin films", J. of Materials Science, 33 (1998), p 4455- 4459.

- S. Simamoto, Y. Sakata, J. Kojima, N. Kume and Y. Tsujimoto, "Lacquered Polymer-Ceramic Composite Dielectric Film for Capacitors", IEEE Intl. Symp. On electrical Insulation, 1992, p 140 – 143.
- E. B. Slamovich and I. A. Aksay, "Structure Evolution in Hydrothermally Processed (<100C) BaTiO₃ Films", J. Am. Ceram. Soc, 79[1], (1996), p 239 –247
- K. Slenes and K. Law, "A polymer-ceramic composite for integrated capacitors",
IMAPS Advanced Technology Workshop in Integrated Passives, Denver, 1998.
- G. Stauf, C. Seegel, R. Watts, and H. O'Bryan, "Modified stoichiometry for integrated RF capacitors",
IMAPS Advanced Technology Workshop on Integrated Passives, Denver, 1998.
- K. Suu, T. Masuda, Y. Nishiyoka and N. Tani, "Preparation of SrBi₂Ta₂O₉ ferroelectric thin film by rf magnetron sputtering", Integr. Ferroelectr., 21,1-4, pt 1, (1998), p. 407-418.
- A. Trigg, "Thin film resistors and capacitors for multichip modules", Proceedings of IEEE 48th ECTC, 1998, pp 228-231.
- M. Tsukada, J. Cross, M. Nishizawa, K. Kurihara, and N. Kamehara, Preparation and characterization of dielectric thin films for decoupling capacitors", Proceedings, ICEMCM, 1995, pp 347-352.
- R. Tummala, E. Rymaszewski, Microelectronics Packaging Handbook, Van Nostrand Reinhold, New York 1989
- K. Vorotilov, M. Yanovskaya, E. Turevskaya and A. Sigov, "Sol-gel derived ferroelectric thin films: avenues for control of microstructural and electric properties", J. Sol Gel Sci. Technol., 16, 1-2, (1999), p 109-118.
- K. Yao, W. Zhu and X. Yao, "Development of Ba-Ti-B Glass-Ceramic thick-film capacitors by sol-gel technology", IEEE Transactions on CPMT –Part C, 21, No. 1, (1998), p 20-25.

